

GIGABYTE GA-8IE2004P-L  
Schematics

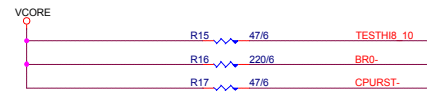
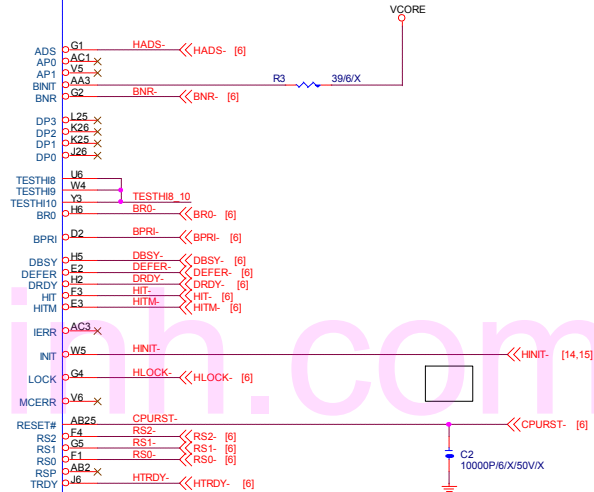
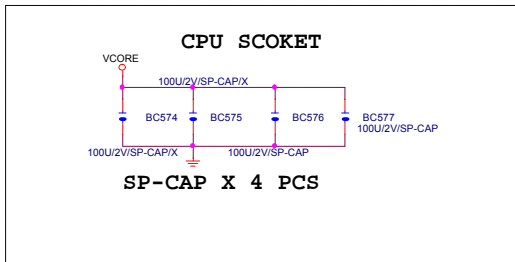
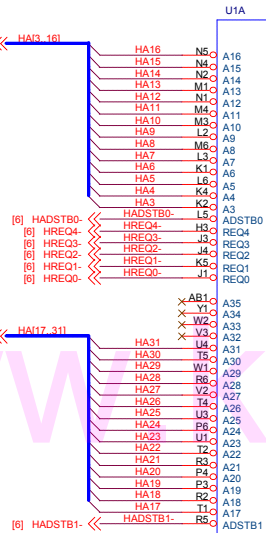
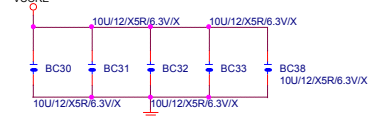
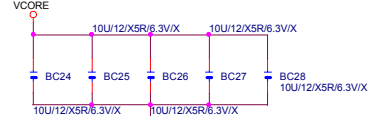
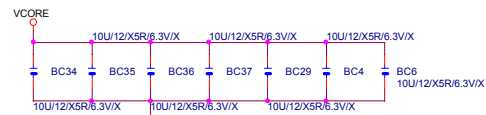
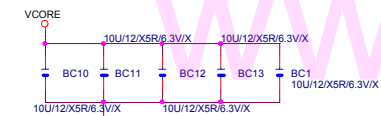
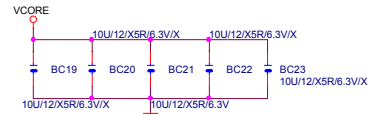
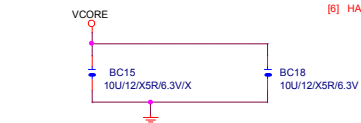
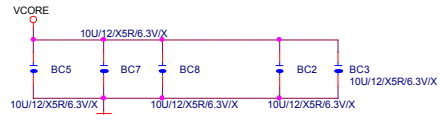
Revision 1.0

SHEET	TITLE
01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	WILLIAMATE_478A
04	WILLIAMATE_478B
05	WILLIAMATE_478C
06	MCH-BROOKDALE-E_A
07	MCH-BROOKDALE-E_B
08	MCH-BROOKDALE-E_C
09	MD0~63
10	DDR1~2
11	DDR-TERM
12	AGP
13	ICH4_1
14	ICH4_2
15	FWH (SINGLE BIOS)
16	ICS950223 CLOCK GEN
17	PCI1_2
18	PCI3_4
19	PCI5
20	ITE LPC I/O
21	IDE
22	KB_PS2

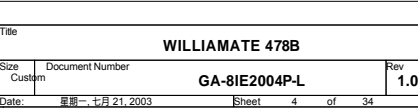
SHEET	TITLE
23	COM_LPT_FDD
24	F-USB1 & F-USB2
25	FPANEL
26	CODEC
27	AUDIO_GAMEPORT
28	AUDIO_SPDIF
29	DDR POWER
30	POWER1
31	POWER2
32	LAN RTL8100C & B-USB CONNECTOR
33	GPIO LIST
34	PCI ROUNT LIST
35	
36	
37	
38	
PCB	4v藍C

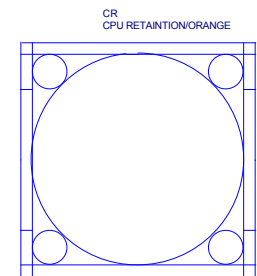
<div><div></div><div></div><div></div><div></div><div></div></div>		COMPONENT SIDE (0.5 oz. Copper) VCC SIDE (1 oz. Copper) GND SIDE (1 oz. Copper) SOLDER SIDE (0.5 oz. Copper)
GIGABYTE		
TitleCOVER SHEET		
Size Custom	Document NumberGA-8IE2004P-L	Rev1.0
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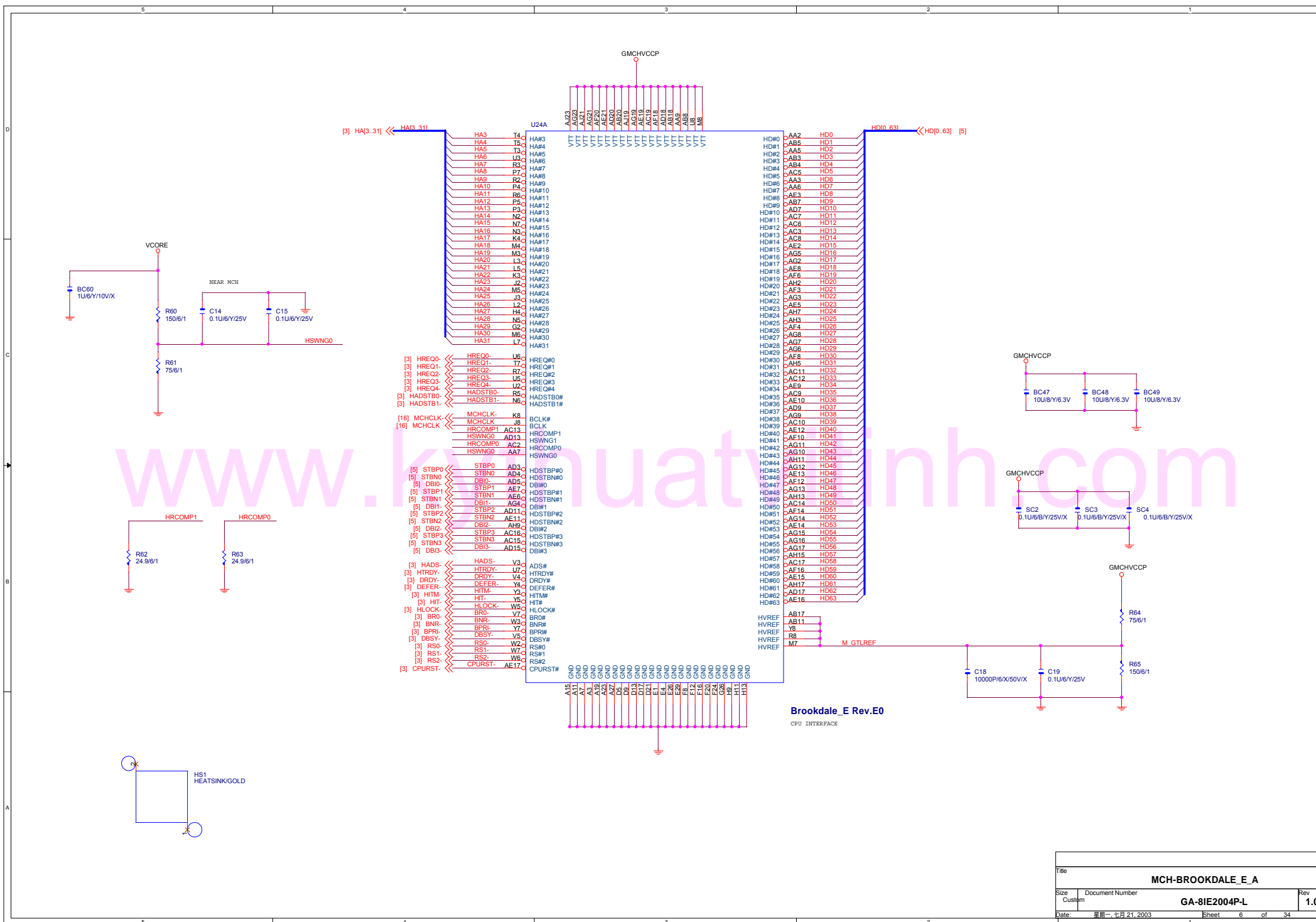
<b>GIGABYTE</b>				
Title <b>BOM &amp; PCB MODIFY HISTORY</b>				
Size Custom	Document Number  <b>GA-8IE2004P-L</b>			Rev  <b>1.0</b>
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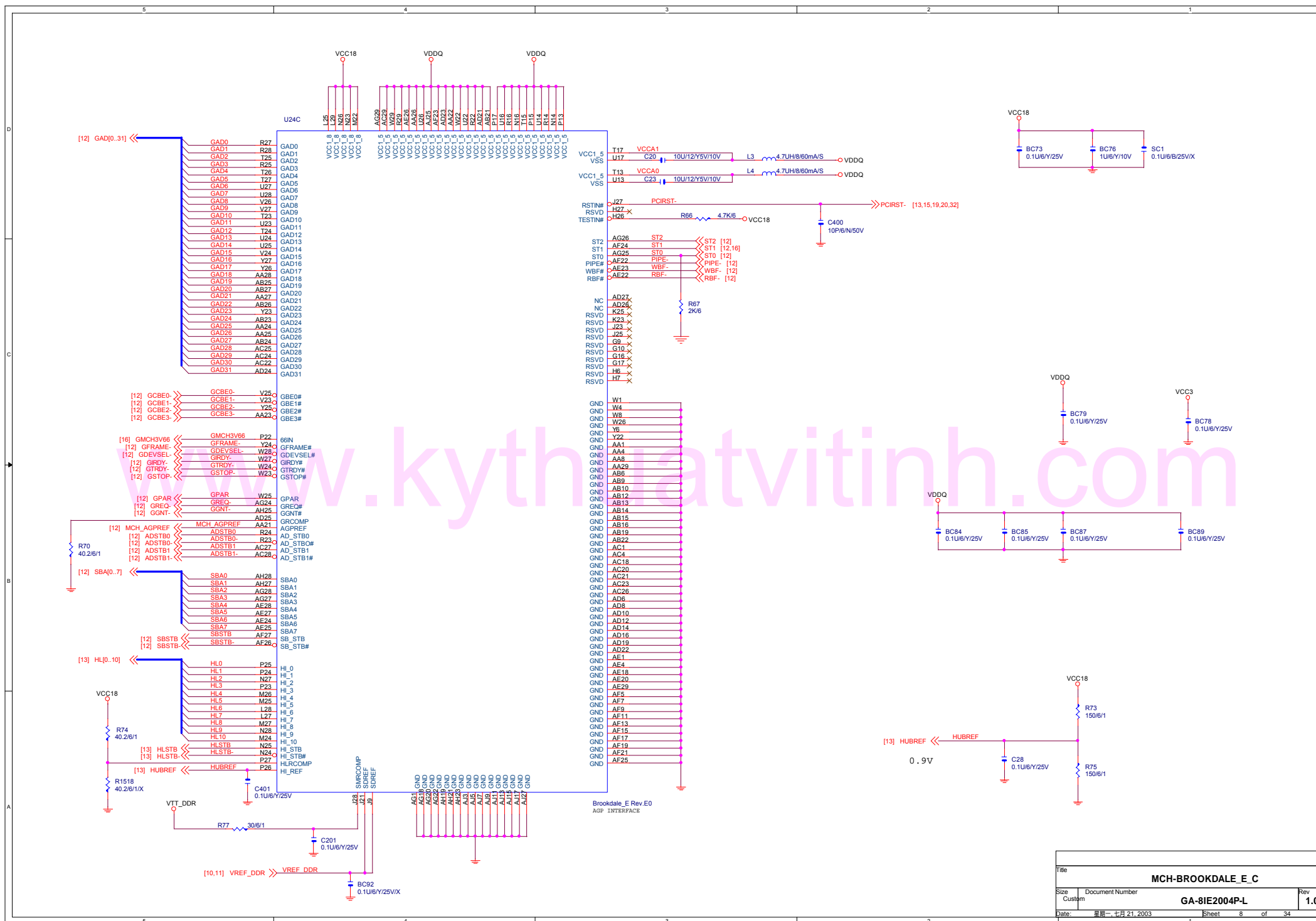
Title		
WILLIAMATE 478A		
Size	Document Number	Rev
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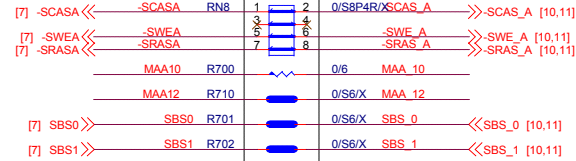
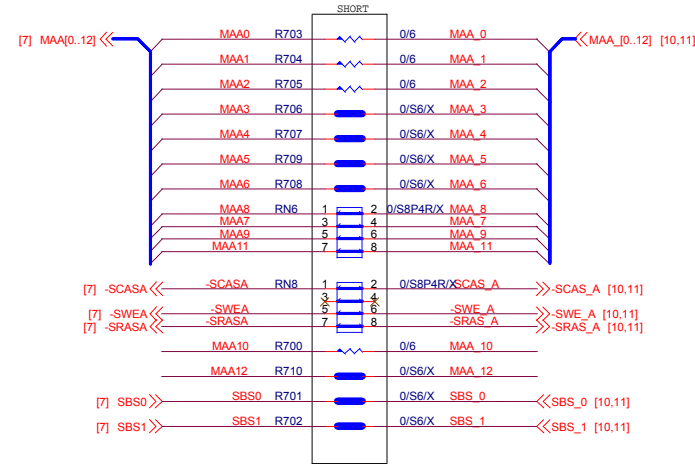
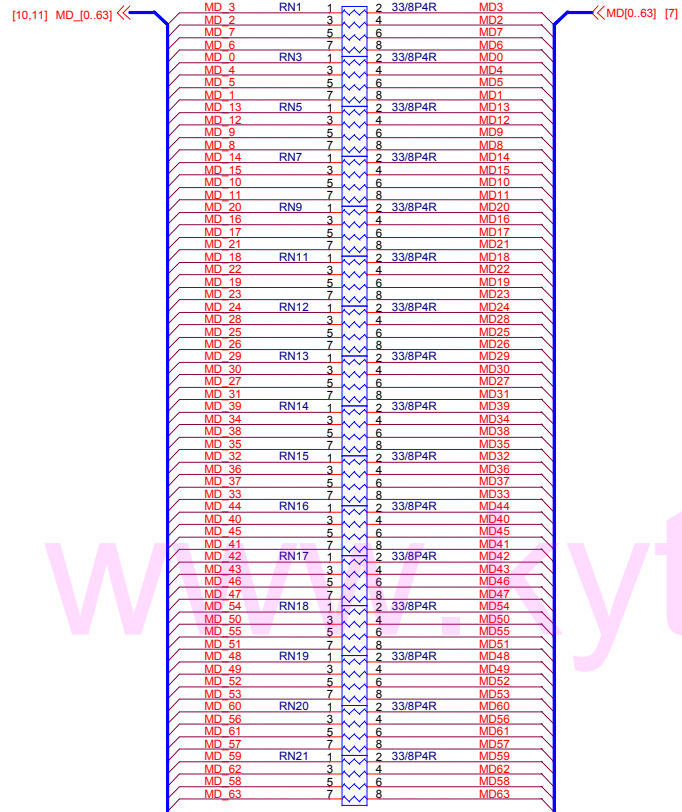






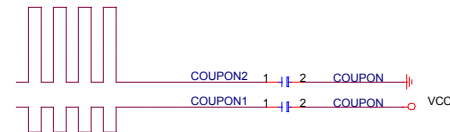
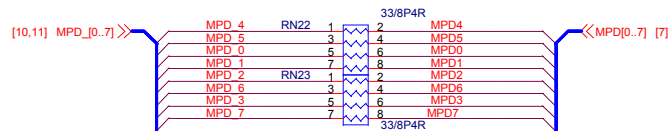
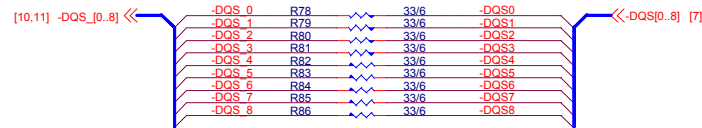
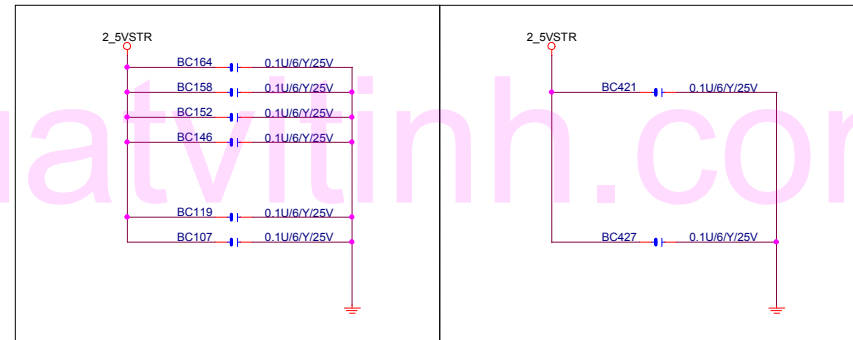
Title				
MCH-BROOKDALE E_C				
Size	Custom	Document Number	Rev	
		GA-8IE2004P-L	1	
Date:	星期一	七月 21, 2003	Sheet	8 of 34

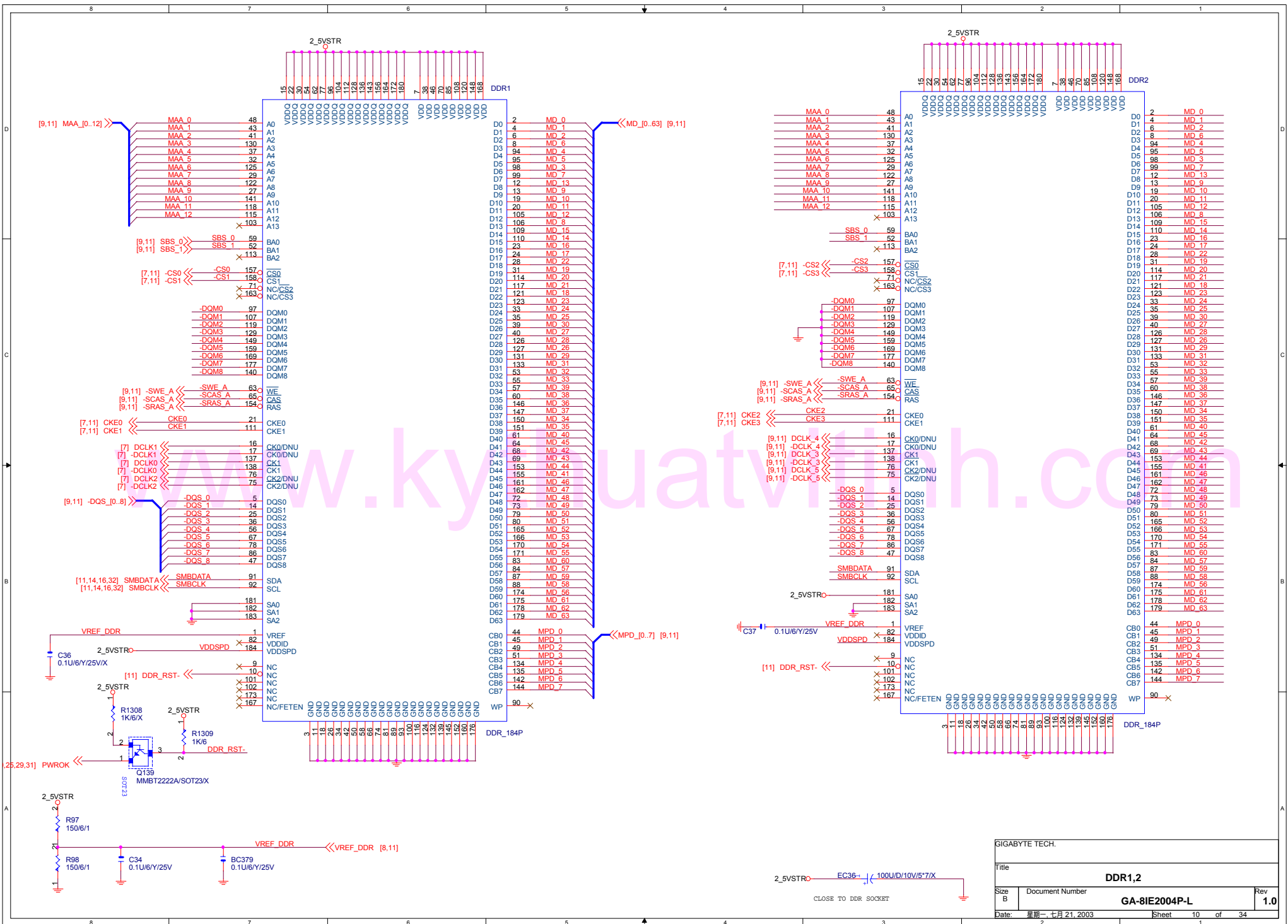


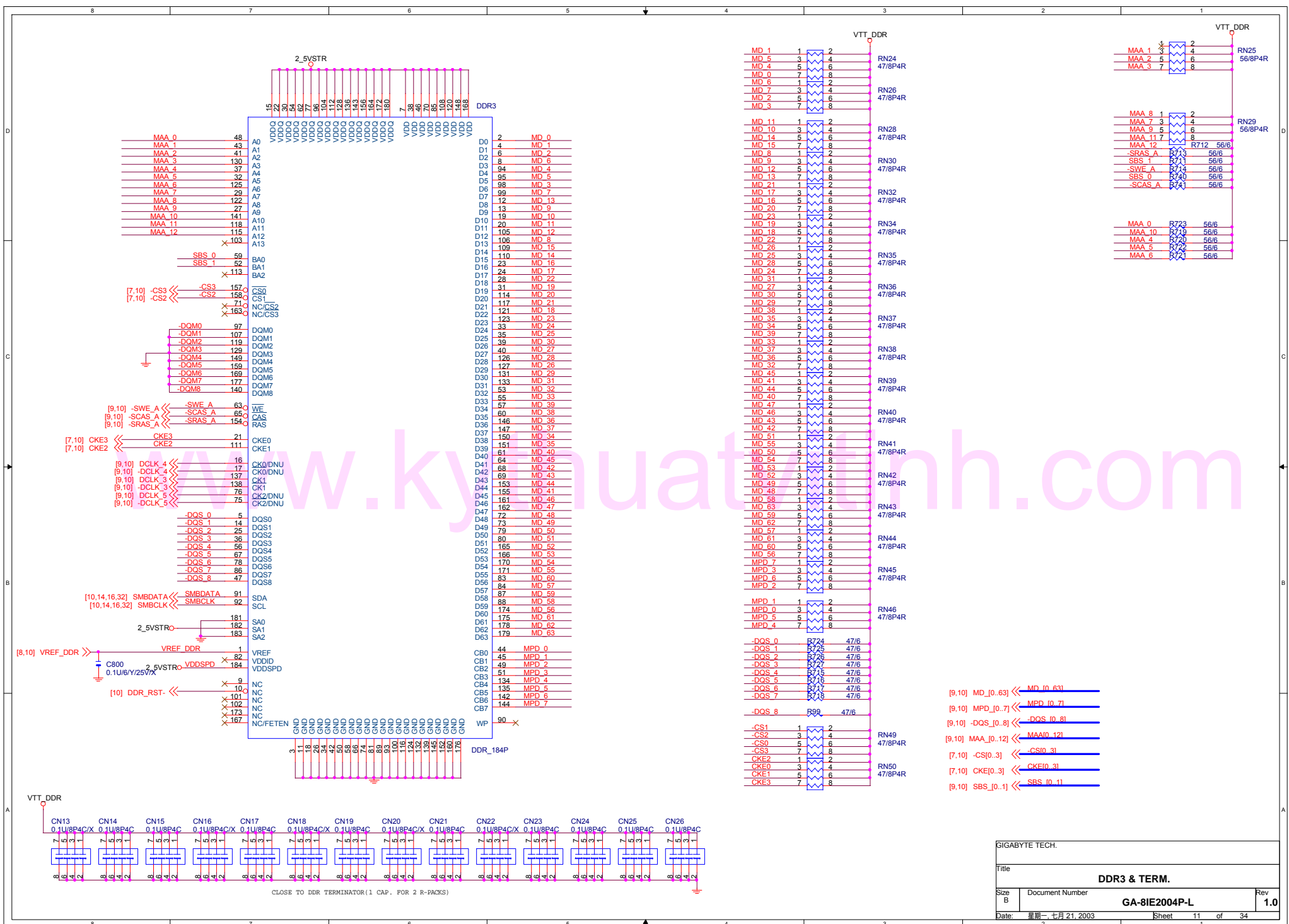


BETWEEN DIMM1 & DIMM2

BETWEEN DIMM2 & DIMM3

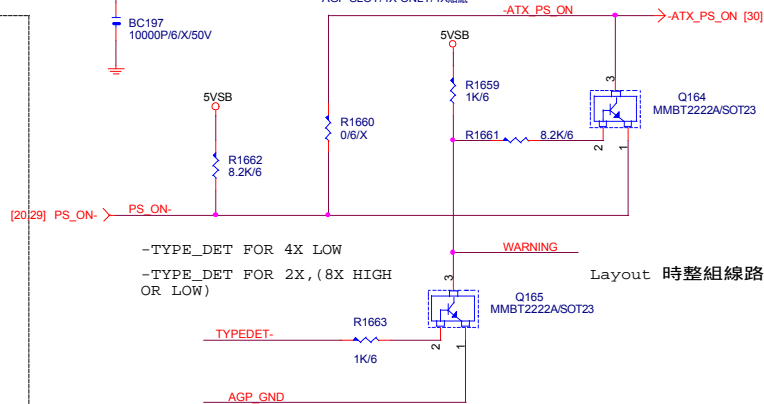
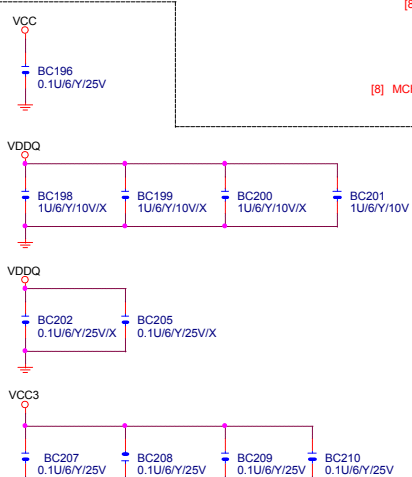
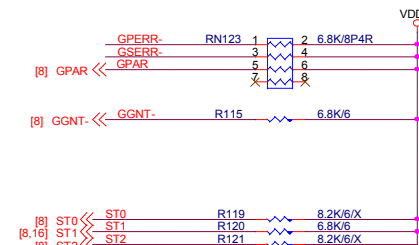
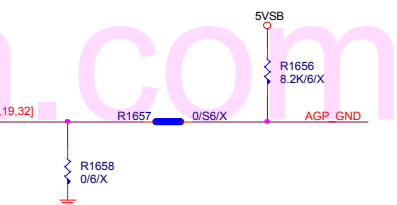
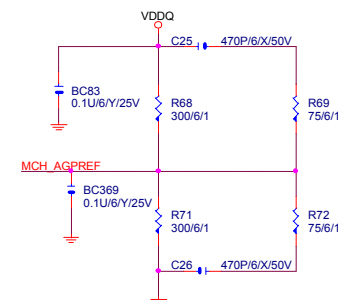
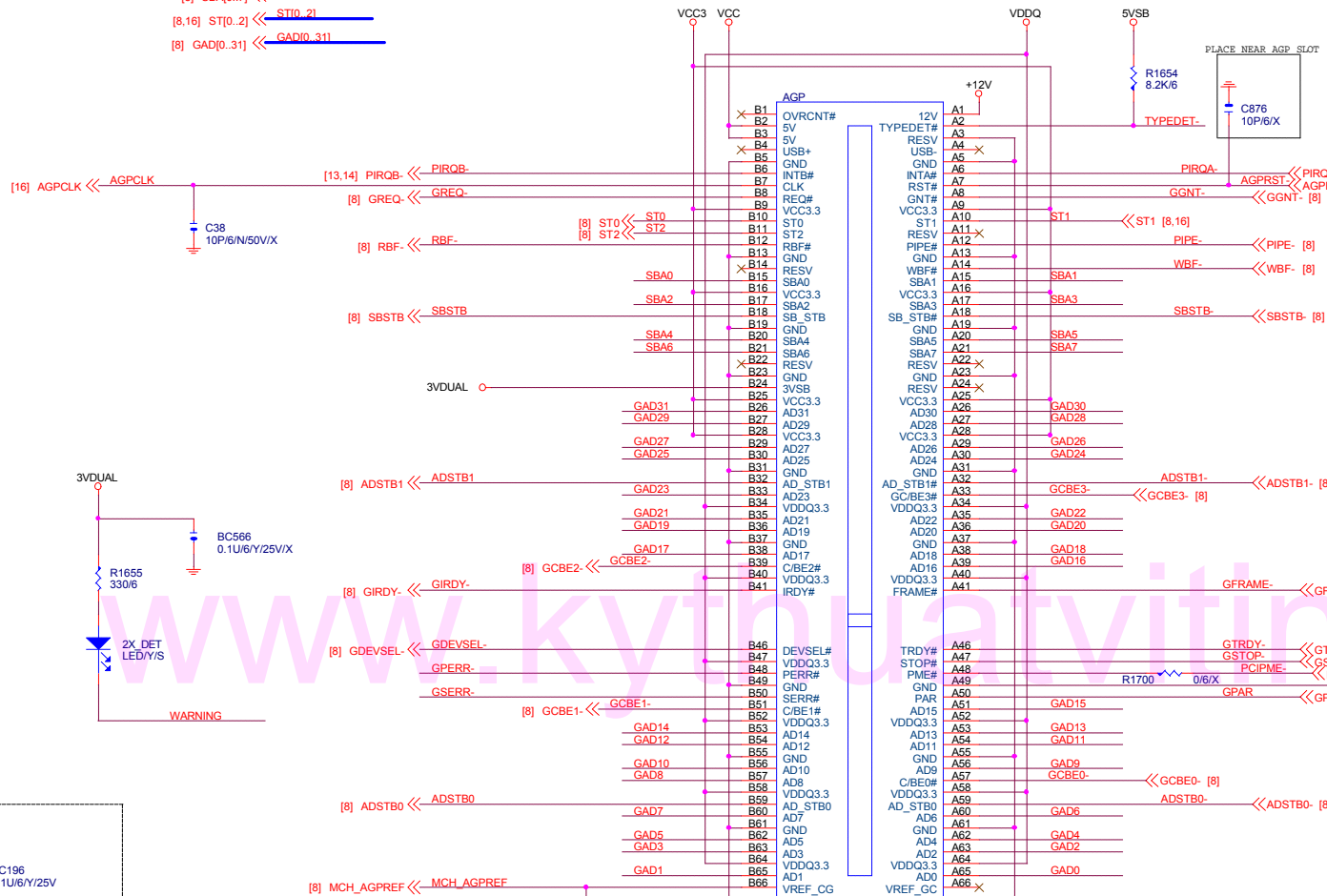






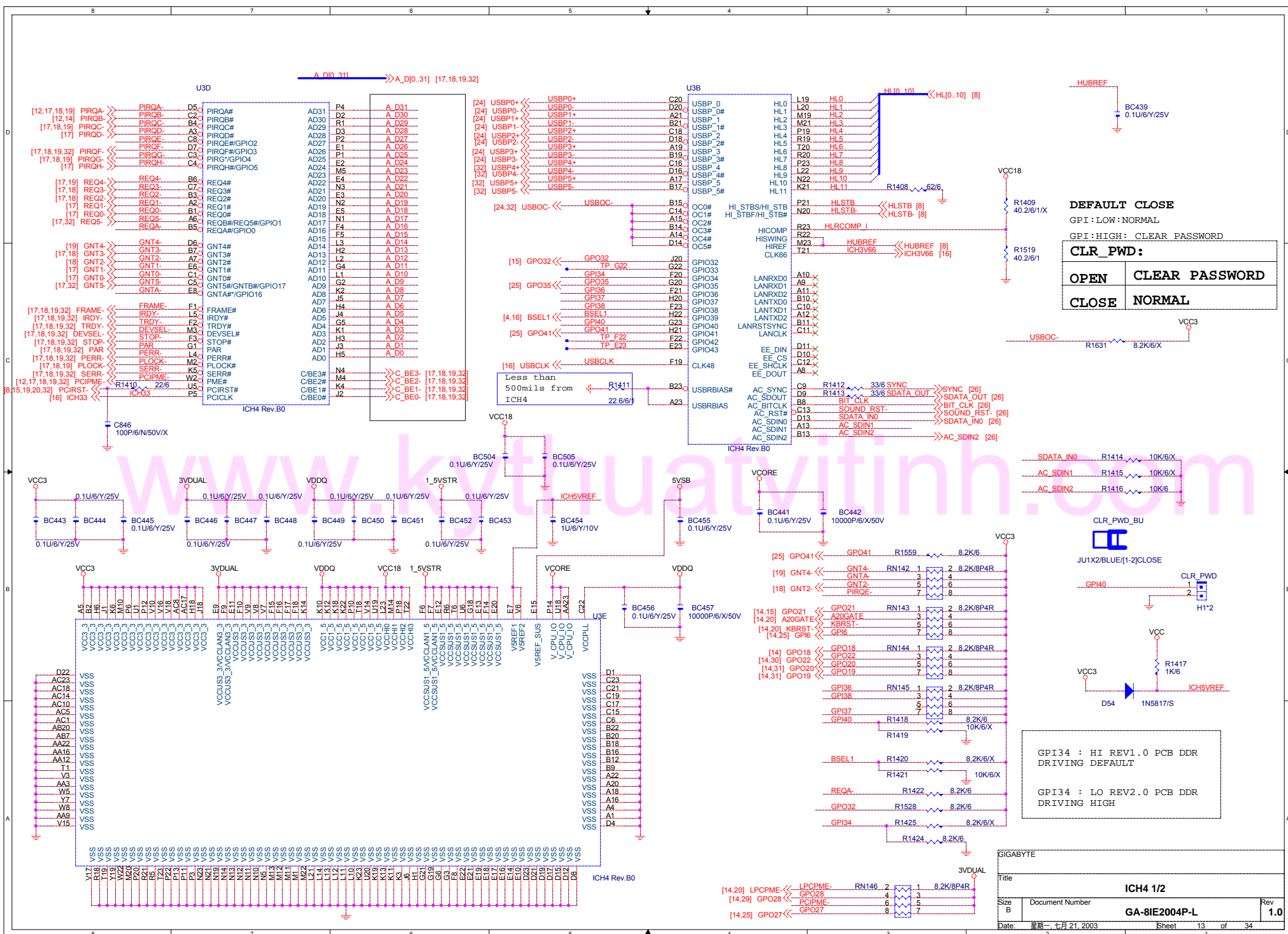
4X only

[8] SBA[0..7] << SBA[0..7]  
[8,16] ST[0..2] << ST[0..2]  
[8] GAD[0..31] << GAD[0..31]



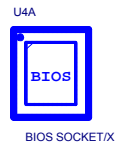
Layout 時整組線路均需靠近 AGP SLOT

GIGABYTE CORP.			
Title			
AGP SLOT			
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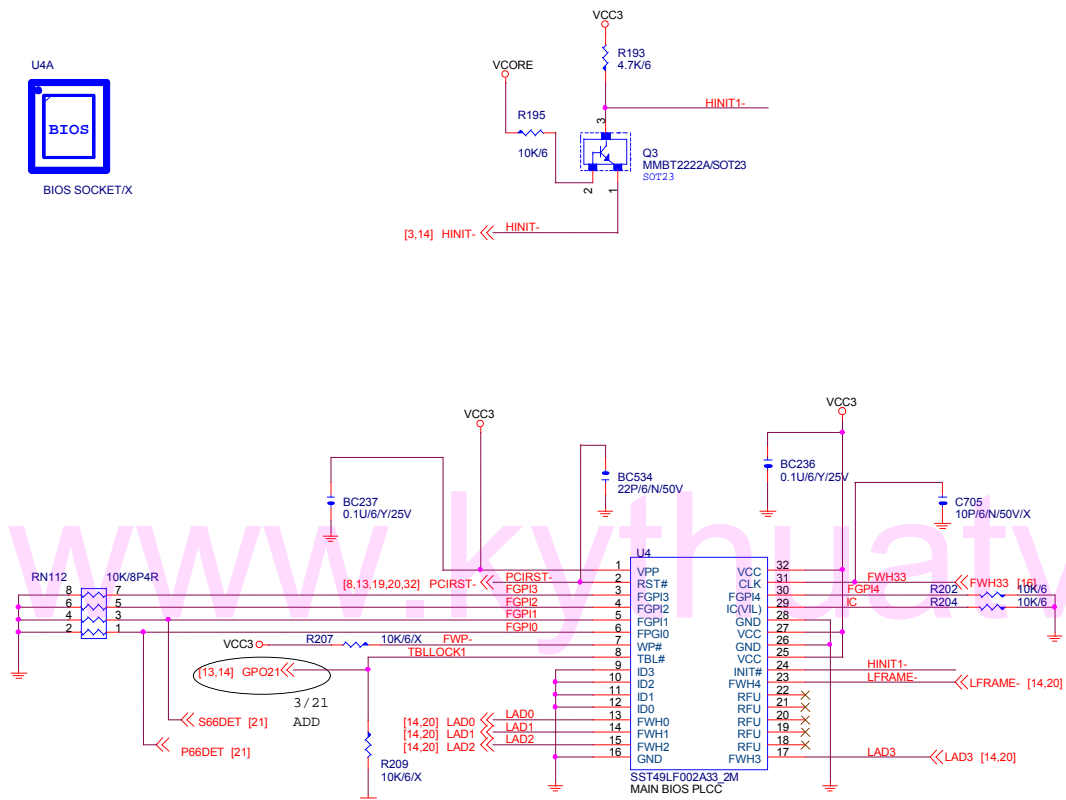








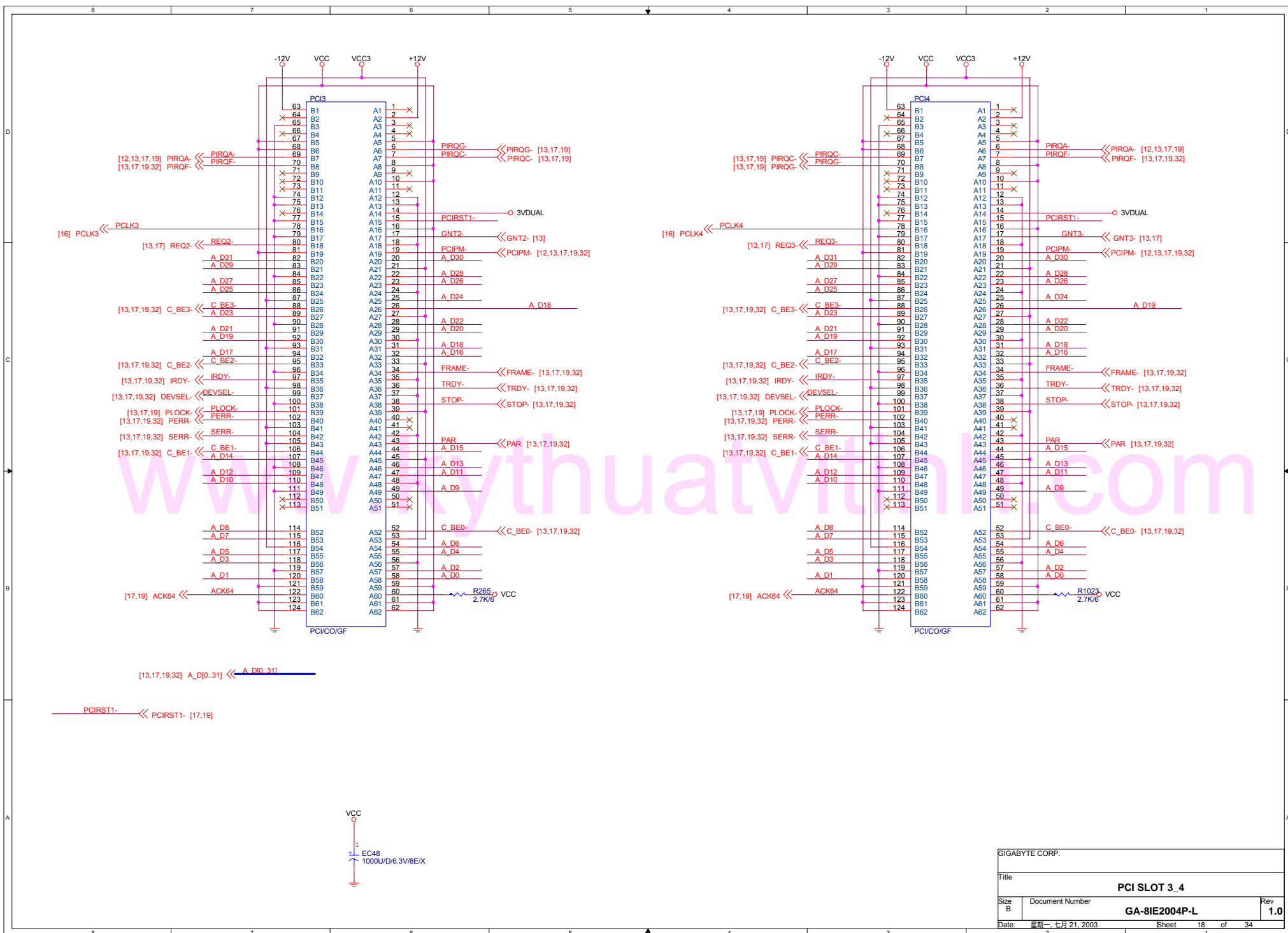
2002/04/15 MODIFY WRITE PROTECT

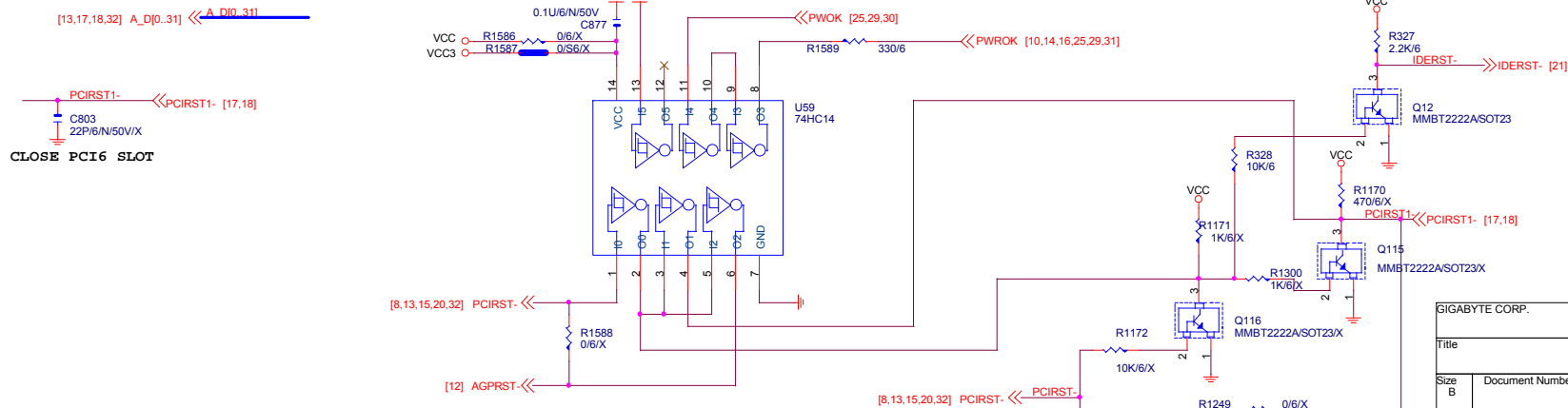
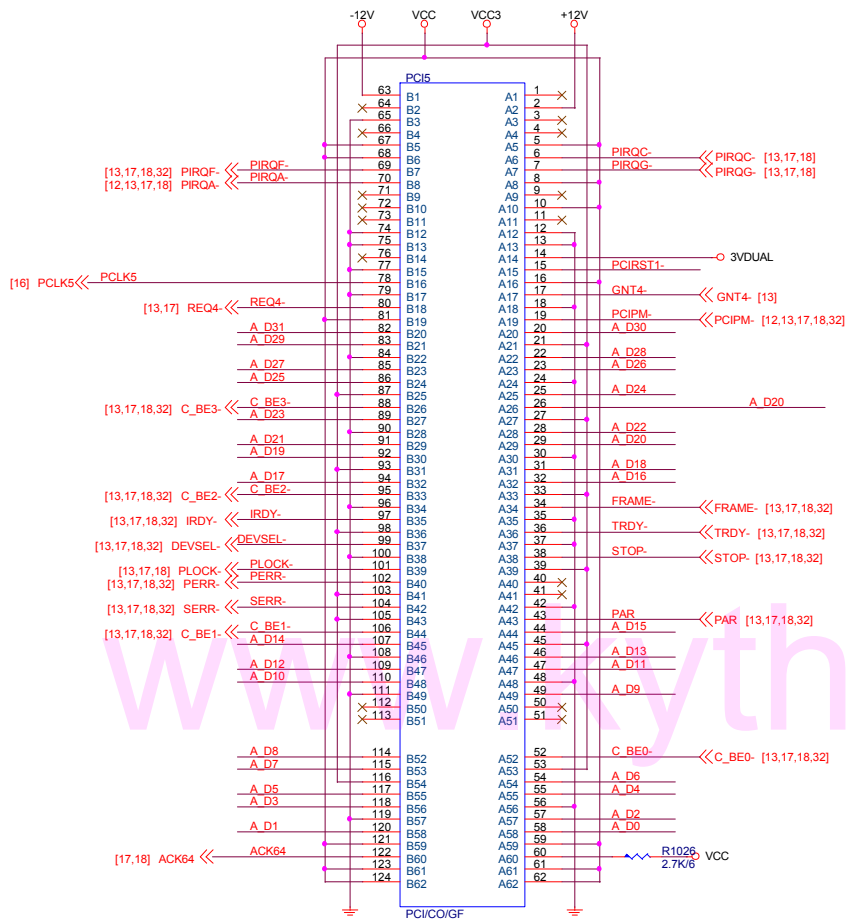




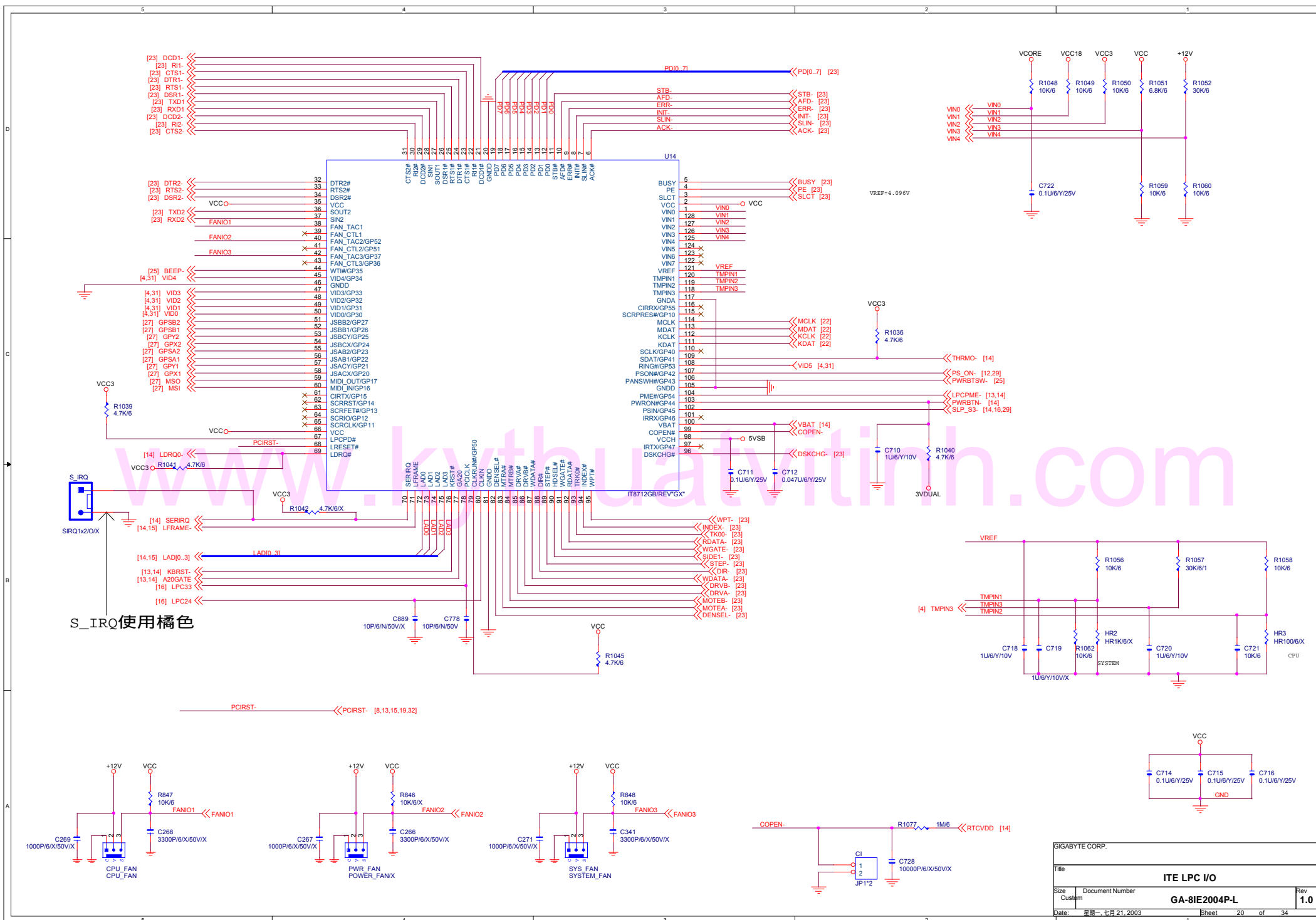


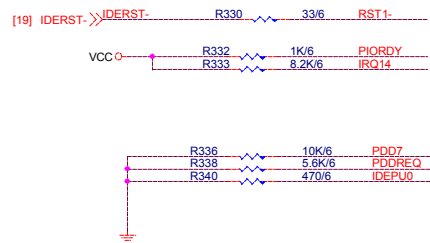
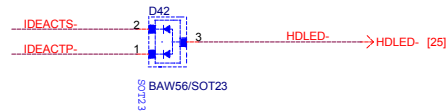




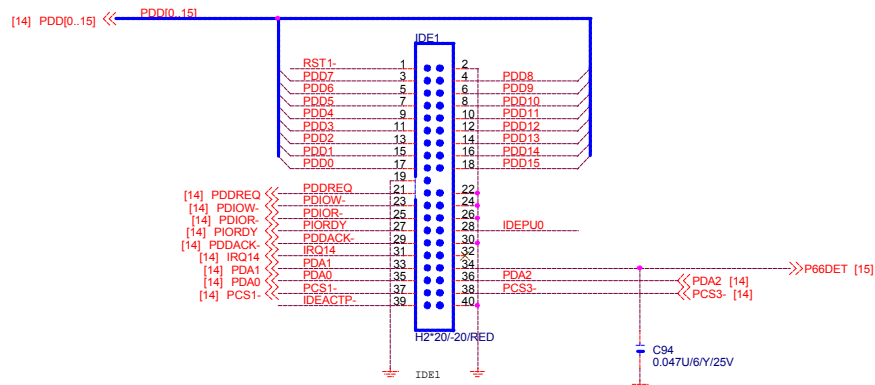


GIGABYTE CORP.		
Title		
PCI SLOT 5		
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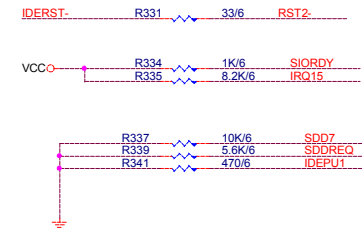




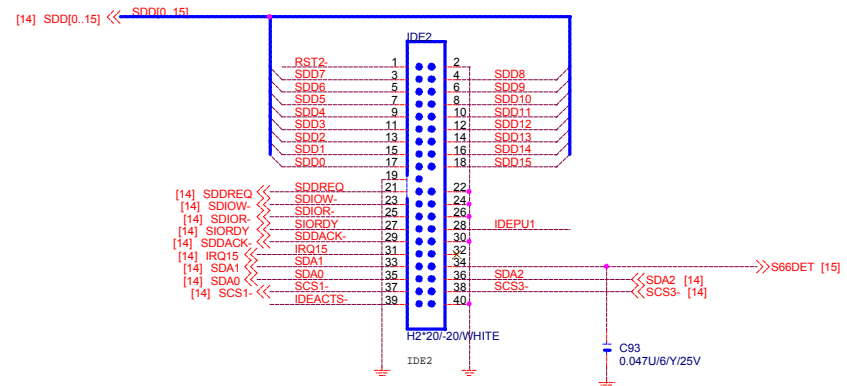
PRIMARY IDE CONNECTOR



BIOS:CABLE DETECT AND DEVICE DETECT



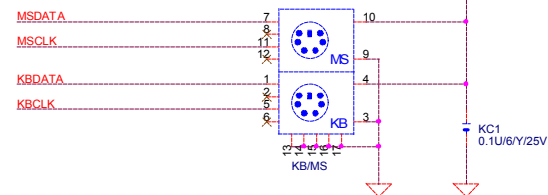
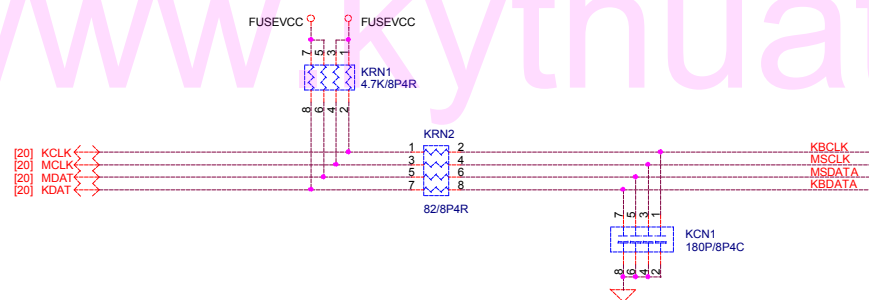
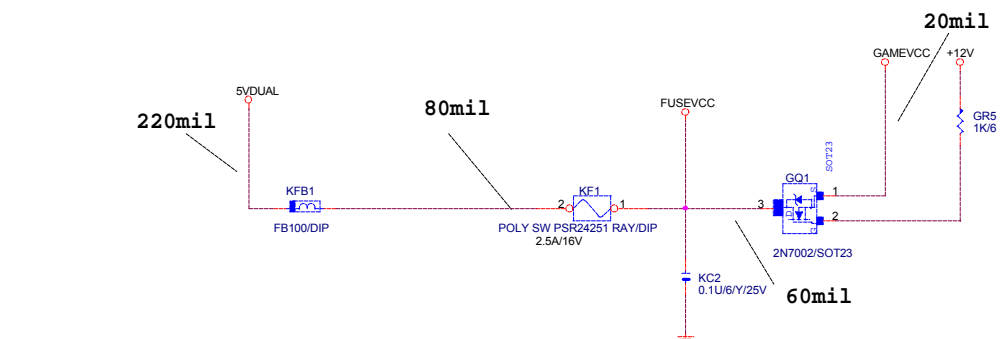
SECONDARY IDE CONNECTOR



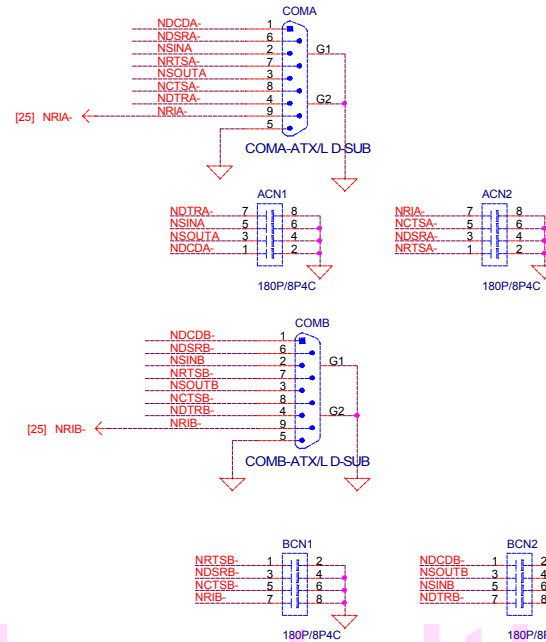
GIGABYTE CORP.

Title			
IDE CONNECTOR			
Size	Document Number	Rev	
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模組化線路

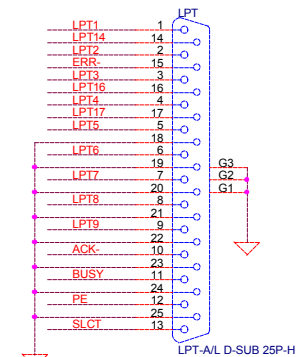
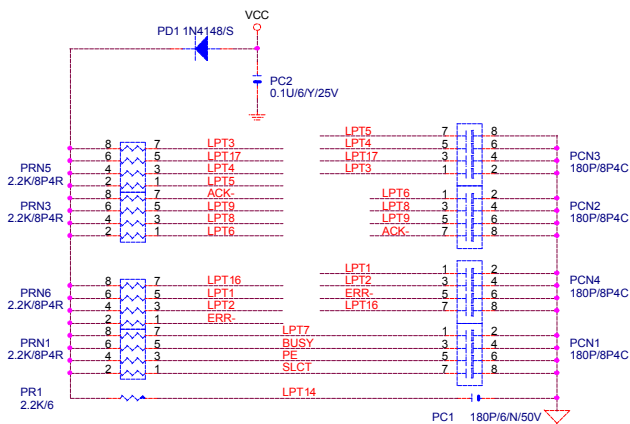


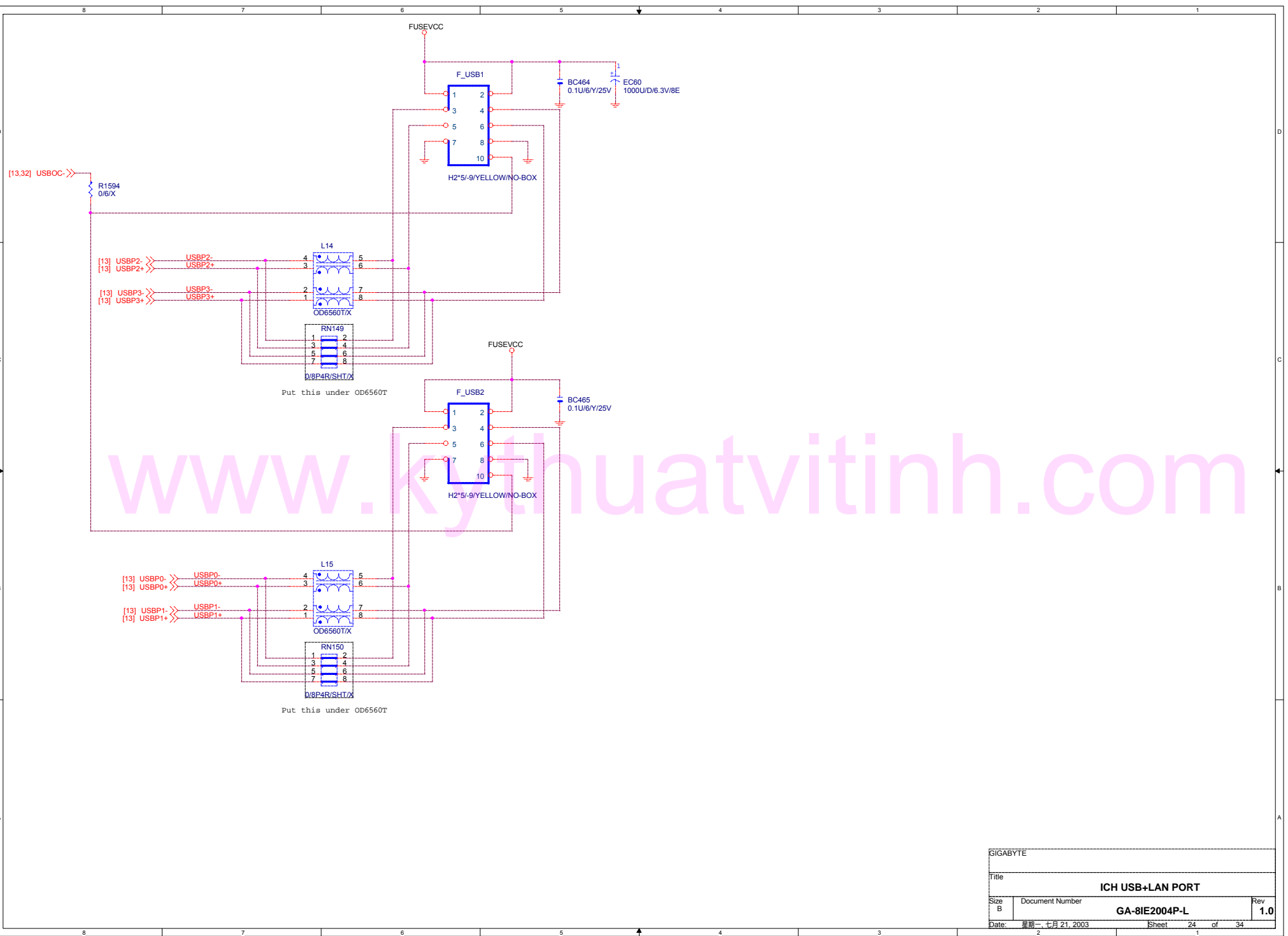
## 模組化線路

[illegible]

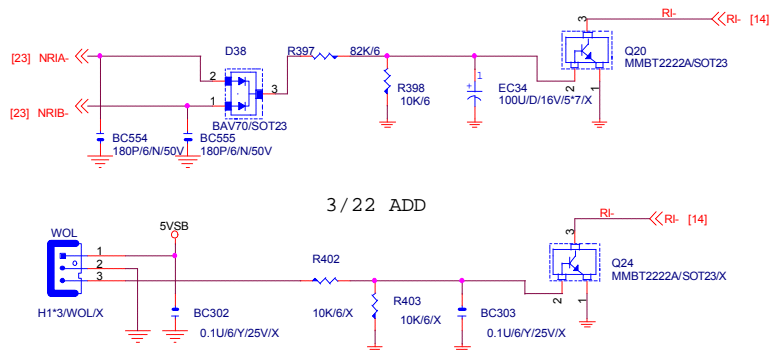
The diagram illustrates the 33/8P4R interface connections for three PRN (Peripheral Resource Number) blocks: PRN7, PRN4, and PRN2. Each PRN block is represented by a blue square with a wavy pattern, indicating a 33/8P4R interface. The connections are as follows:

- PRN7:**
  - Input [20] AFD- connects to AFD- (pin 1).
  - Input [20] STB- connects to STB- (pin 3).
  - Input [20] PD0 connects to PD0 (pin 5).
  - Input [20] INIT- connects to INIT- (pin 7).
  - Output LPT14 (pin 2) connects to LPT1.
  - Output LPT1 (pin 4) connects to LPT2.
  - Output LPT2 (pin 6) connects to LPT16.
- PRN4:**
  - Input [20] SLIN- connects to SLIN- (pin 1).
  - Input [20] PD2 connects to PD2 (pin 3).
  - Input [20] PD3 connects to PD3 (pin 5).
  - Output LPT3 (pin 2) connects to LPT17.
  - Output LPT17 (pin 4) connects to LPT4.
  - Output LPT4 (pin 6) connects to LPT5.
- PRN2:**
  - Input [20] ERR- connects to ERR- (pin 1).
  - Input [20] ACK- connects to ACK- (pin 3).
  - Input [20] BUSY- connects to BUSY- (pin 5).
  - Input [20] PE connects to PE (pin 7).
  - Output LPT6 (pin 2) connects to LPT8.
  - Output LPT8 (pin 4) connects to LPT9.
  - Output LPT9 (pin 6) connects to LPT7.

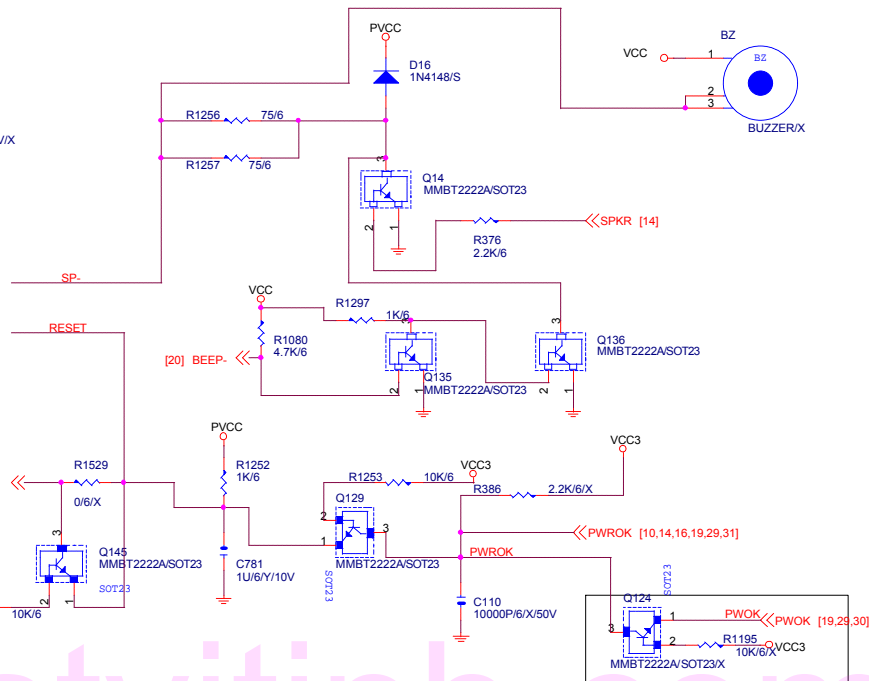
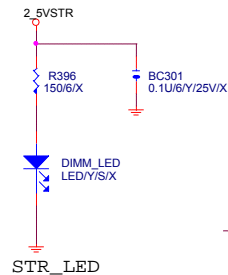








3 / 22 ADD



### 3 PIN POWER LED

LED	1	2	3
MPD+	1	2	3
MPD-	1	2	3
MPD-	1	2	3
P_LED_1X3			

### States for green LED

LED States	ACPI States	GPO28
ON	S1, S3	0
OFF	S0, S5	1

NO1 GPO35 只需在S1 PROGRAMMING LOW

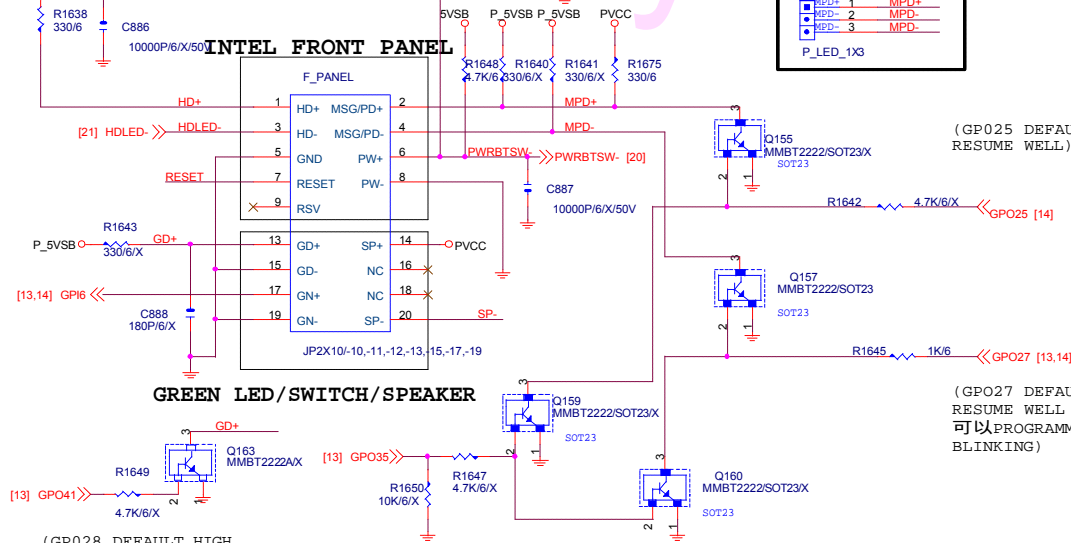
### States for a single-color power LED

LED States	ACPI States	GPO25	GPO27	GPO35
OFF	S1, S3, S5	1	1	NO1
Steady Green	S0	0	1	0
Blinking Green	S0 (message waiting)	0	B	0

### States for a dual-color power LED

LED States	ACPI States	GPO25	GPO27	GPO35
OFF	S5	1	1	X
Steady Green	S0	0	1	0
Blinking Green	S0 (message waiting)	0	B	0
Steady Yellow	S1, S3	1	0	NO1
Blinking Yellow	S1, S3 (message waiting)	1	B	NO1

### INTEL FRONT PANEL



### GREEN LED/SWITCH/SPEAKER

(GPO28 DEFAULT HIGH, RESUME WELL)

(GPO35 DEFAULT HIGH, MAIN POWER)

(GPO25 DEFAULT HIGH, RESUME WELL)

(GPO27 DEFAULT HIGH, RESUME WELL AND 可以PROGRAMMING BLINKING)

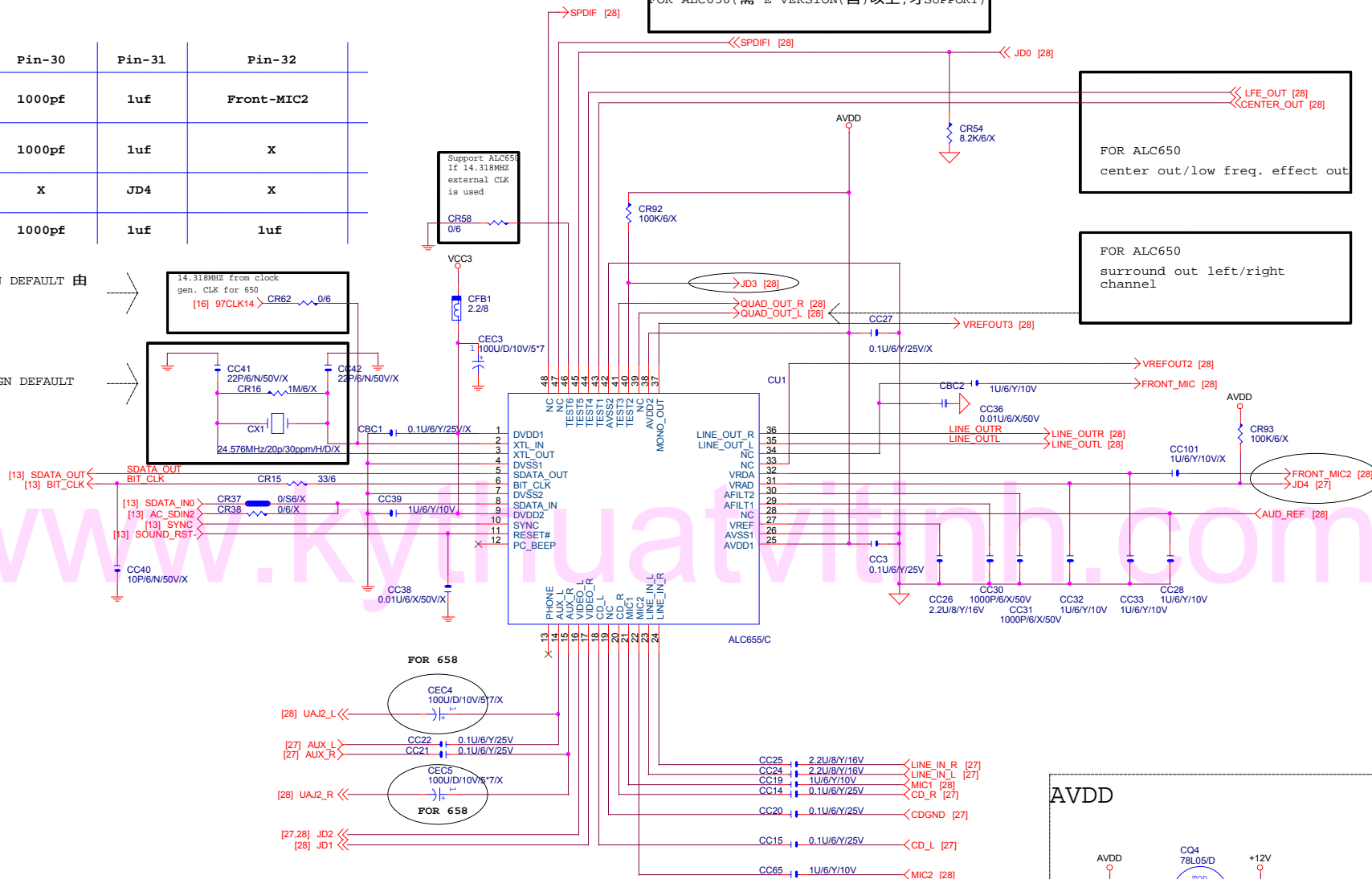
GIGABYTE

Title			
PANEL & STR LED & RI			
Size B	Document Number	Rev	
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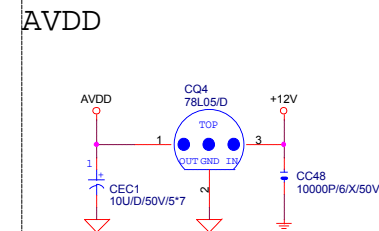
### Filter Cap design:

	Pin-29	Pin-30	Pin-31	Pin-32	
ALC655 Rev D	1000pf	1000pf	1uf	Front-MIC2	
ALC655 Rev C	1000pf	1000pf	1uf	X	
ALC658	X	X	JD4	X	
ALC650	1000pf	1000pf	1uf	1uf	

14.318MHZ from clock  
gen. CLK for 650  
[16] 97CLK14 CR62 0/6



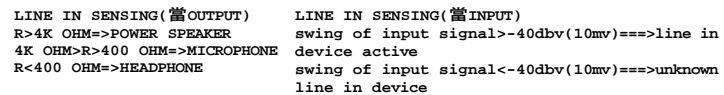
	Pin-45(JD0)	Pin-17(JD1)	Pin-16(JD2)	Pin-40(JD3)	Pin-31(JD4)
ALC655	for MIC-IN	for FRONT-OUT	for LINE-IN		
ALC658	for MIC-IN	for UAJ1	for UAJ2	for FRONT-OUT External pull high is needed	for LINE-IN External pull high is needed



GIGABYTE CORP.

Title			
AC97			
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模組化線路



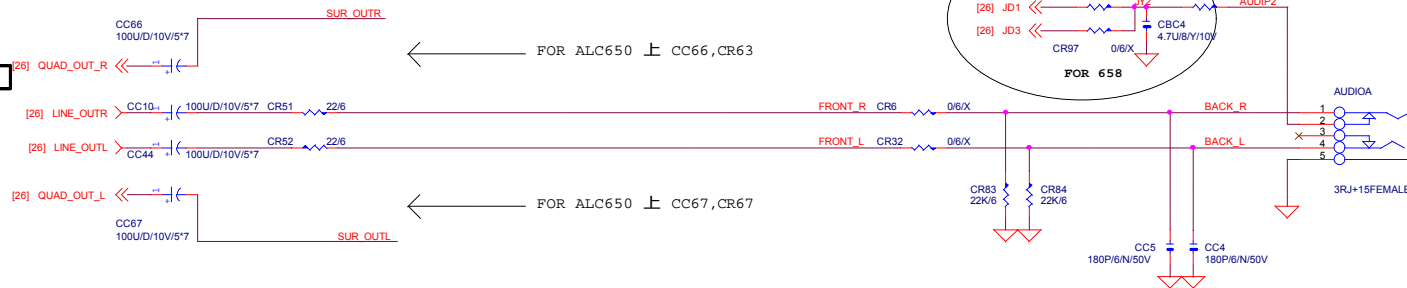
The schematic shows a blue header labeled "CDIN\*1'4 HEADER[BLACK]" with four pins numbered 1 through 4. Pin 1 is connected to "[26] CD\_L ←". Pin 2 is connected to "[26] CD\_R ←". Pin 3 is connected to "[26] CDGND ← CDGND". Pin 4 is connected to a common ground point. This common point branches to three capacitors: CC16 (1000P/6/X/50V/X), CC37 (1000P/6/X/50V/X), and CC12 (1000P/6/X/50V/X). Each capacitor is connected to ground. A note at the bottom right specifies: "1000P/6 FOR EMI", "10K/6 FOR DC LOOP".

## 模組化線路

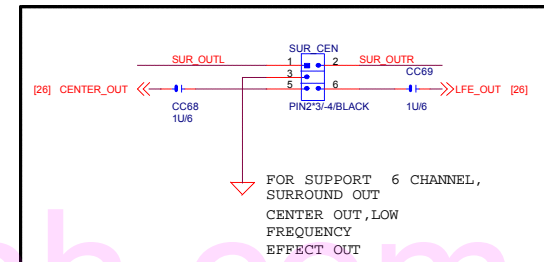
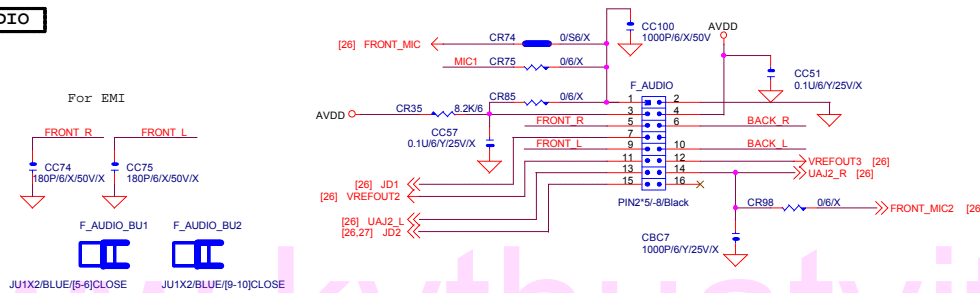
JDO,JD2,GPIQ0 為偵測DEVICE INPUT 時由LOW TO HIGH Edge trigger(pop manual)

1/2(3.14)RC=1/2(3.14)8.2K\*4.7U=4.3HZ以上AC 信號全部衰減 TO 0V  
不會造成JDO 誤動作(無device 時play wav )

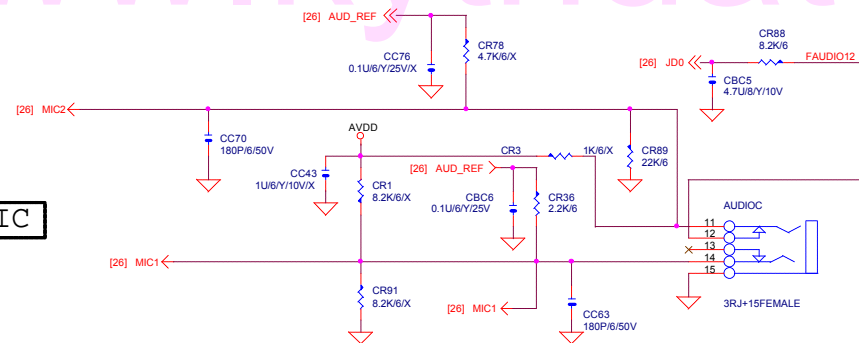
## LINE OUT



## INTEL FRONT AUDIO



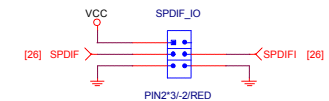
## MIC



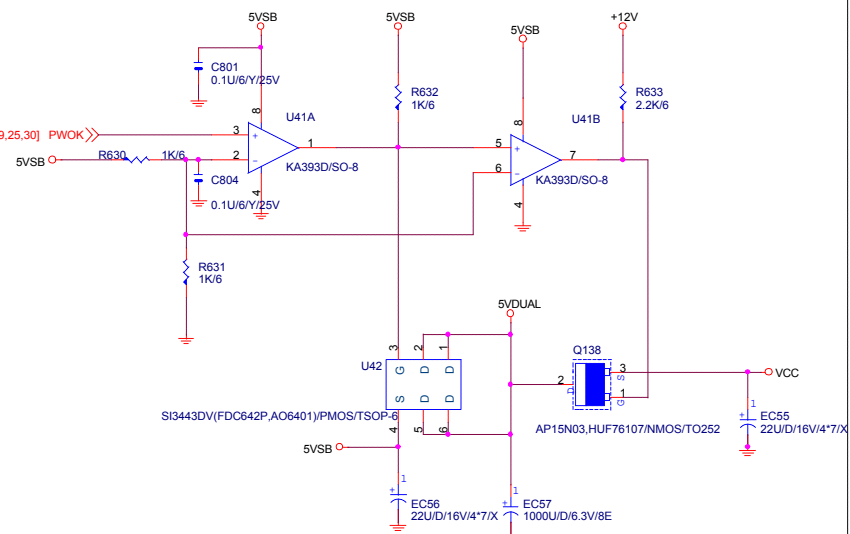
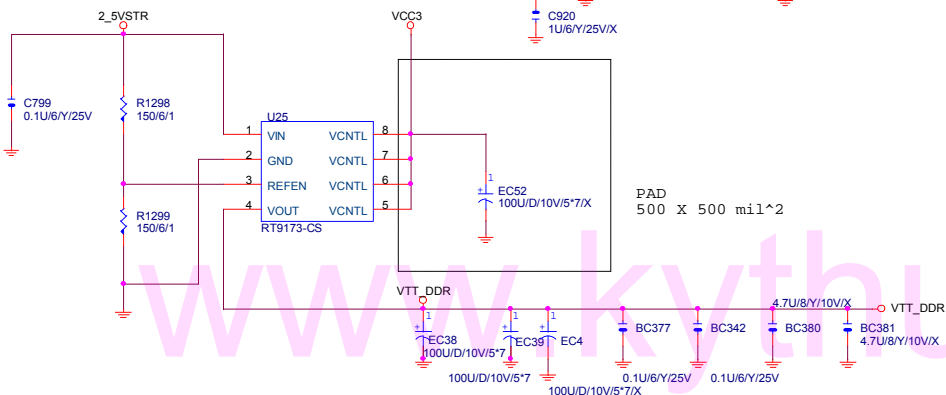
MICROPHONE IN SENSING(當INPUT)(利用vref 偏壓  
與CR43,CR32 並聯求出阻抗)  
7.1k ohm>R>2.3k ohm==>microphone in  
R<2.3k ohm or R>7.1k ohm==>unknown device

MICROPHONE IN SENSING(當OUTPUT)  
R>4K OHM=>POWER SPEAKER  
4K OHM>R>400 OHM=>MICROPHONE  
R<400 OHM=>HEADPHONE

## SPDIF\_IO



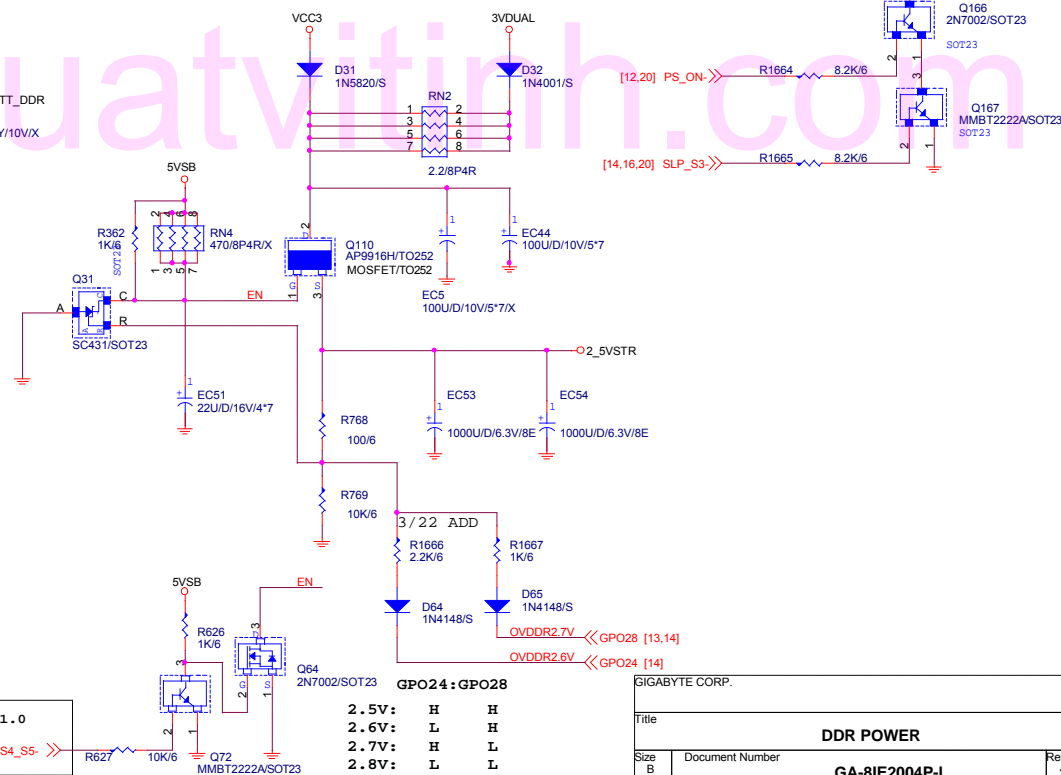
# 1.25V VTT\_DDR LINEAR SOLUTION



5VDUAL CIRCUIT

Northwood: +1.45V  
Prescott: +1.225V

Big Copper  
to GND



REV1.0

[14,25] S4\_S5- >>

GIGABYTE CORP.

Title  
DDR POWER

Size B Document Number GA-8IE2004P-L Rev 1.0

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**CPU Voltage ID output**

VCC3

RN1511 2 1K/8P4R VID3

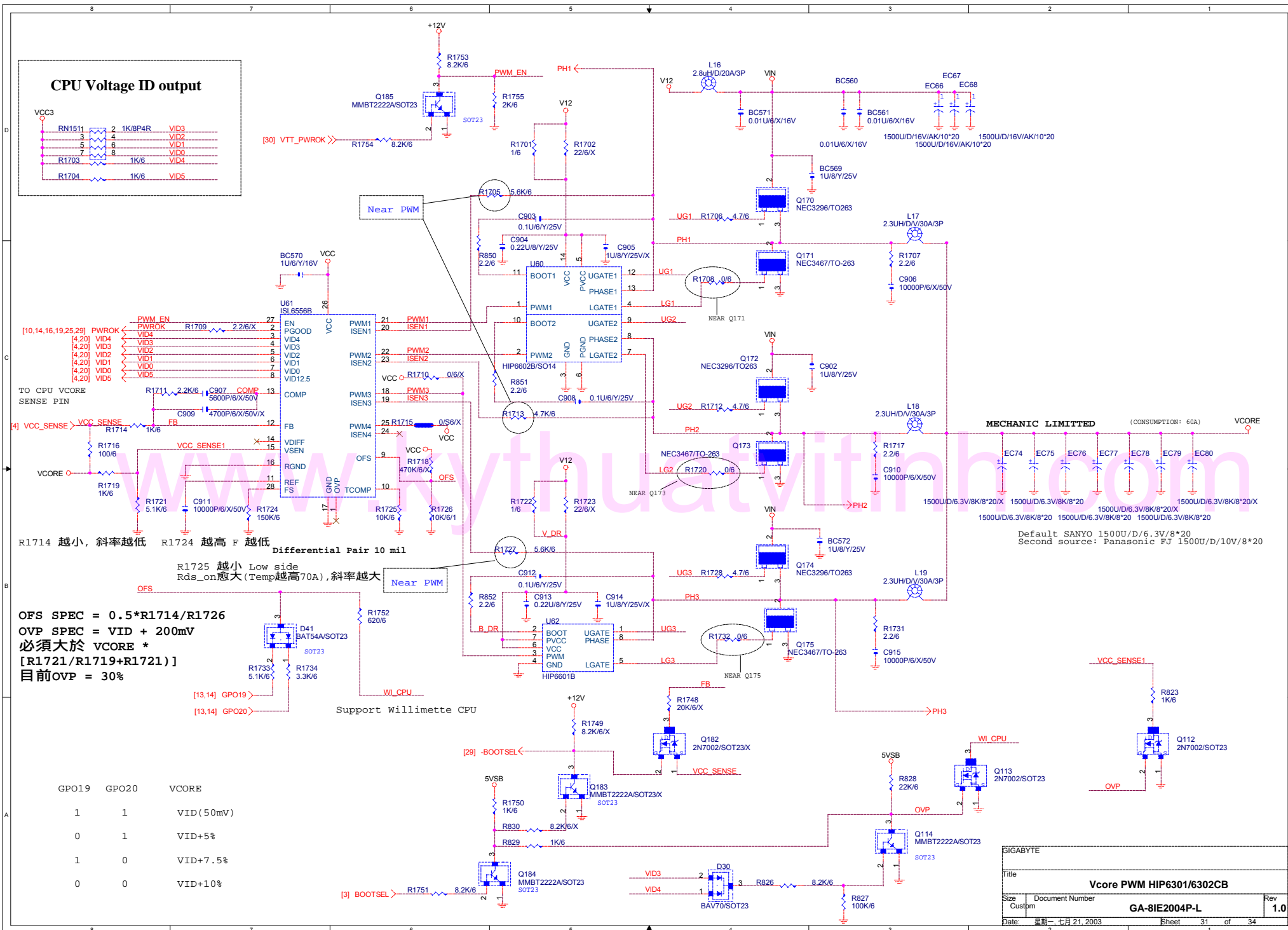
3 4 VID2

5 6 VID1

7 8 VID0

R1703 1K/6 VID4

R1704 1K/6 VID5



GIGABYTE				
Title				
Vcore PWM HIP6301/6302CB				
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LU1:  
100M:RTL8100C

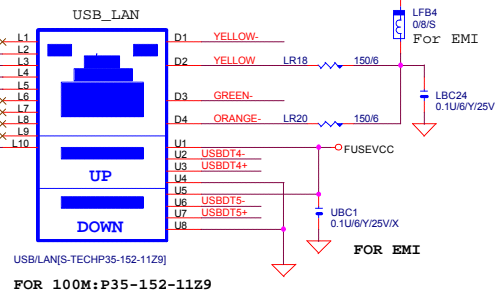
LR15:  
100M:5.9K/6/1



IRDY- [13,17,18,19]  
FRAME- [13,17,18,19]  
C BE2- [13,17,18,19]

LR22, LR23, LBC26 Close to Lan Chip  
Realtek suggestion (TX+, TX-).

LR24, LR25, LBC27 Close to Lan Chip  
Realtek Suggestion (RX+, RX-).

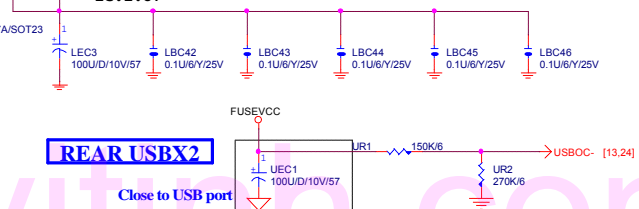


FOR 100M:P35-152-11Z9

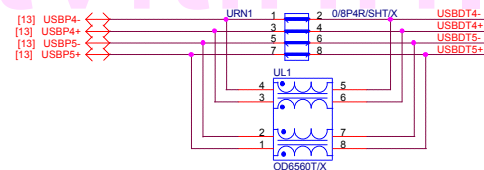
The diagram shows two power supply rails. The top rail, labeled **3VDUAL**, has a decoupling capacitor **LEC1** (100u/D/10V/57) connected to ground. It then branches out to seven pins, each with a decoupling capacitor: **LBC1** (0.1u/6V/25V), **LBC2** (0.1u/6V/25V), **LBC3** (0.1u/6V/25V), **LBC4** (0.1u/6V/25V), **LBC5** (0.1u/6V/25V), **LBC6** (0.1u/6V/25V), and **LBC7** (0.1u/6V/25V). A blue box labeled **POWER DECOUPLING CAP.** highlights the LBC capacitors. The bottom rail, labeled **DVDD**, has four decoupling capacitors: **LBC11** (0.1u/6V/25V), **LBC12** (0.1u/6V/25V), **LBC37** (0.1u/6V/25V), and **LBC38** (0.1u/6V/25V).

LQ3:  
100M:2N2907A  
1G:N/A

DVDD:  
100M:2.5V  
1G:1.8V



Close to USB port



**When Inetl & GBT Gigabit (8110S)**  
**Note: LEDS1-0 must set to 00 in EEPROM**

<b>GIGABYTE</b>			
Title			
<b>LAN RTL8100C</b>			
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# GIGABYTE GA-8IE2004P-L GPIO LIST

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SHEET

TITLE

GPI		
GPI0/REQA-	NA	PULL 8.2K TO VCC3
GPI1/REQ5-		PULL 2.7K TO VCC
GPI2/PIRQE-	ID	PULL 8.2K TO VCC3 (default)
GPI3/PIRQF-		PULL 8.2K TO VCC3
GPI4/PIRQG-		PULL 8.2K TO VCC3
GPI5/PIRQH-	ID	PULL 8.2K TO VCC3 (default)
GPI6		PULL 8.2K TO VCC3 (GREEN BUTTON)
GPI7		PULL DOWN 10K TO GND
GPI8	ID	PULL 8.2K TO VCC3 (default)
GPI9	NA	NOT IMPLEMENTED
GPI10	NA	NOT IMPLEMENTED
GPI11		PULL 4.7K TO 3VDUAL (SMBALERT)
GPI12/LPCPME-		PULL 8.2K TO 3VDUAL (PME-)
GPI13		NC
GPI14	NA	NOT IMPLEMENTED
GPI15	NA	NOT IMPLEMENTED

SHEET

TITLE

GPO		
GPO16	NA	PULL 8.2K TO VCC3(CAN'T PULL DOWN )因為會decode bios address 不正確:FF
GPO17		PULL 8.2K TO VCC3 (GNT5-)
GPO18	NA	PULL 8.2K TO VCC3 此OUTPUT 會TOGGLE.(在開機時).BIOS POST OK
GPO19		PULL 8.2K TO VCC3
GPO20		PULL 8.2K TO VCC3
GPO21		PULL 8.2K TO VCC3 (TOP BLOCK)
GPO22		PULL 8.2K TO VCC3
GPO23		PULL 8.2K TO VCC3
GPO24		PULL 4.7K TO 3VDUAL
GPO25		PULL 4.7K TO 3VDUAL (POWER LED)
GPO26		NOT IMPLEMENTED
GPO27		PULL 8.2K TO 3VDUAL (POWER LED)
GPO28		PULL 8.2K TO 3VDUAL
GPO32		PULL 8.2K TO 3VDUAL (BIOS WRITE PROTECT )
GPO35		PULL DOWN 10K TO GND (POWER LED)

COMPONENT SIDE (0.5 oz. Copper)	
VCC SIDE (1 oz. Copper)	
GND SIDE (1 oz. Copper)	
SOLDER SIDE (0.5 oz. Copper)	
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SHEET

[illegible]

SHEET

TITLE

[illegible][illegible]